data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon an error frequency within one of said plurality of data storage registers reaching a predetermined frequency, and wherein said processor drives outputs a signal to an external unit upon a remaining amount of said storage capacity reaching a predetermined remaining capacity, and wherein said signal is representative of said remaining amount of said storage capacity.

23. The memory unit of claim 22, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining capacity, wherein each of the comparisons produces a result, and wherein said processor outputs said result to said external unit.

24. The memory unit of claim 22, wherein said processor output said signal to said external unit upon said number of wrote operations performed to a respective of said addresses in said main memory reaching a predetermined number.

REMARKS

Claims 1-12 are pending. By this Amendment, claims 1-12 are canceled, and new claims 13-24 are added.

Rejections -- 35 USC §102

Claims 1-12 stand rejected under 35 USC §102(e) as being anticipated by Yamagami et al. (U.S. Patent No. 6,130,837). Claims 1-12 have been canceled by the present amendment. Claims 13-24 have been added to more clearly define the scope of the invention. Care has been taken to ensure that claims 13-24 present no new matter and are supported by the originally filed specification.

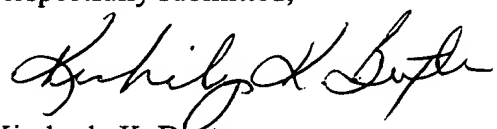
Particularly, claims 13-24 have been amended to more clearly reflect that the present invention includes the feature of displaying the remaining available capacity of the spare memory as well as the feature of displaying the correspondence between the remaining available capacity of the spare memory and a predetermined remaining capacity. Claims 16 and 22 include the feature of transferring data to the spare memory in response to an error frequency.

Yamagami et al. (U.S. Patent No. 6,130,837) does not teach or suggest the features noted above. Rather, Yamagami teaches that the number of writing operations at each flash memory is counted (by a number of erasures management table) in order to flag the flash memory, to which the erasing operations have been performed many times, and in order to perform the writing operations to the other flash memory, so that the number of writing operates to the flash memories can be averaged. Further, Yamagami teaches that the buffer memory (for the purpose of temporary storage), an error memory (including an error information area, a usage information area and a substitutive memory area), and a data memory are provided as a memory means. According to the data of the error information area, the data memory is used when the data memory has been determined to be a normal condition, or the substitutive memory area is used when the data memory has been determined to be an abnormal condition.

In view of the foregoing, it is submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of the application are respectfully requested.

The Examiner is invited to telephone the undersigned if the Examiner believes it would be useful to advance prosecution.

Respectfully submitted,



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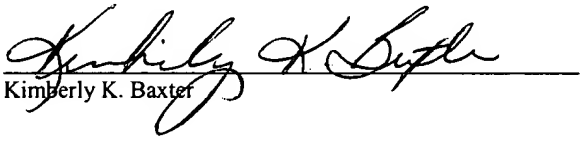

Kimberly K. Baxter

ATTACHMENT
REDLINED AMENDMENT

Claims As Amended

Please cancel claims 1-12 without prejudice or disclaimer.

Please add new claims 13-24 as follows:

1. (Canceled) A memory unit having a memory, a memory status indicator and a processor, wherein the processor monitors the status of the memory and communicates memory status information to the memory status indicator.

2. (Canceled) A memory unit as set forth in Claim 1, wherein the memory status indicator is a display, an external display or at least one indicator light.

3. (Canceled) A memory unit as set forth in Claim 2, wherein the processor monitors write operations in the memory and determines when the number of write operations reaches a pre-determined number.

4. (Canceled) A memory unit as set forth in Claim 2, wherein the processor monitors remaining available capacity in the memory and determines when the remaining available capacity is less than a pre-determined amount.

5. (Canceled) A memory unit as set forth in Claim 2, wherein the processor monitors error frequency in the memory and determines when the error frequency reaches a pre-determined number.

6. (Canceled) A method of determining and indicating memory status, comprising the steps of: calculating a value representative of memory usage;

comparing the calculated number with a pre-determined number; and changing a memory status indicator when the calculated number reaches the pre-determined number.

7. (Canceled) A method as in claim 6, wherein calculating a value representative of memory usage comprises the step of calculating a total number of write operations performed in a memory.

8. (Canceled) A method as in claim 7 further comprising the step of transferring data stored in a memory location to a spare memory area when the calculated value of the respective address of the memory reaches the pre-determined number.

9. (Canceled) A method as in claim 6, wherein calculating a value representative of memory usage comprises the step of calculating error frequency in a memory.

10. (Canceled) A method as in claim 9 further comprising the step of transferring data stored in a memory location to a spare memory area when the calculated value of the respective address of the memory reaches the pre-determined number.

11. (Canceled) A method as in claim 6, wherein calculating a value representative of memory usage 10 comprises the step of calculating remaining available capacity in a memory.

12. (Canceled) A method as in claim 11 further comprising the step of transferring data stored in a memory location to a spare memory area when the calculated value of the respective address of the memory reaches the pre-determined number.

Please add new claims 13-24 as follows:

--13. A memory unit comprising:

a memory having a main memory area and a spare memory area, wherein said main memory area includes a plurality of data storage registers and wherein each of said data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon a number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined value, and wherein said processor drives said display to display a remaining amount of said storage capacity in said spare memory upon a remaining amount of said storage capacity reaching a predetermined remaining capacity.

14. The memory unit as in claim 13, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining capacity, wherein the comparison produces a plurality of different results, and wherein said

processor drives said display in different manners dependent upon said plurality of different results.

15. The memory unit as in claim 13, wherein said processor drives the display upon said number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined number.

16. A memory unit comprising:

a memory having a main memory area and a spare memory area, wherein said main memory area includes a plurality of data storage registers and wherein each of said data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon an error frequency within one of said plurality of data storage registers reaching a predetermined frequency, and wherein said processor drives said display to display a remaining amount of said storage capacity in said spare memory upon a remaining amount of said storage capacity reaching a predetermined remaining capacity.

17. The memory unit of claim 16, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining

capacity, wherein the comparison produces a plurality of different results, and wherein said processor drives said display in different manners dependent upon said plurality of different results.

18. The memory unit of claim 16, wherein said processor drives the display upon said error frequency reaching a predetermined frequency.

19. A memory unit comprising a main memory area and a spare memory are, wherein said main memory area includes a plurality of data storage registers and wherein each of data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored under each of said addresses of said main memory area to said spare memory area upon a number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined value, and wherein said processor outputs a signal to an external unit upon a remaining amount of said storage capacity reaching a predetermined remaining capacity, and wherein said signal is representative of said remaining amount of said storage capacity.

20. The memory unit of claim 19, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining

capacity, wherein each of the comparisons produces a result, and wherein said processor outputs said result to said external unit.

21. The memory unit of claim 19, wherein said processor outputs said signal to said external unit upon said number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined number.

22. A memory unit comprising:

a memory having a main memory area and a spare memory area, wherein said main memory area includes a plurality of data storage registers and wherein each of said data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon an error frequency within one of said plurality of data storage registers reaching a predetermined frequency, and wherein said processor drives outputs a signal to an external unit upon a remaining amount of said storage capacity reaching a predetermined remaining capacity, and wherein said signal is representative of said remaining amount of said storage capacity.

23. The memory unit of claim 22, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining

capacity, wherein each of the comparisons produces a result, and wherein said processor outputs said result to said external unit.

24. The memory unit of claim 22, wherein said processor output said signal to said external unit upon said number of wrote operations performed to a respective of said addresses in said main memory reaching a predetermined number.--